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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/038,469 | 01/03/2002 | Henrik I. Johansen | 42P10695 | 8106 |

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| EXAMINER | |
|---|---|
| AMIN, NIRAV S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2115 | |

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/038,469 | JOHANSEN ET AL. | |
| | Examiner | Art Unit | |
| | Nirav S Amin | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7,12,15,19 and 25* is/are rejected.

7)☒ Claim(s) *2-6,8-11,13,14,16-18,20-24 and 26-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Nguyen et al. (US Patent no. 5,872,959) herein after referred to as Nguyen.

As per claim 7, Nguyen discloses an apparatus comprising a first device (18) to transmit a plurality of data signals in parallel format [Column 3, lines 17-19], a second device (20) to receive the plurality of data signals from the first device, wherein the second device detects phase information [Column 3, lines 21-23] of each data signal with respect to a corresponding clock signal and adjusts a delay of the respective data signal based on the phase information detected prior to sampling of the data signals [Column 2, lines 1-5].

As per claim 15, Nguyen discloses transmitting a plurality of data signals from a first device (18) to a second device (20) in parallel mode [Column 3, lines 18-19] over a first bus [Column 2, lines 8-10], detecting at the second device, phase information [Column 3, lines 21-23] of each data signal with respect to a corresponding clock signal and adjusting a delay of the respective data signal prior to sampling of the data signal at the second device [Column 2, lines 1-5].

Claims 1, 12, 19 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Liu et al. (US Patent no. 6,725,390) herein after referred to as Liu.

As per claim 1, Liu discloses an apparatus comprising a first device (502) to transmit a plurality of data signals [Column 4, lines 55-56] in parallel mode [Column 1, lines 46-47] and a second device (506) coupled to receive the plurality of data signals from the transmitter circuit [via data bus (504), Column 7, lines 21-26], wherein the second device detects phase information of each data signal against a corresponding clock signal [Column 7, lines 35-38] and feeds back the phase information to the first device [Column 7, lines 42-47], the first device adjusts an output delay of each data signal based on the phase information fed back from the second device [Column 7, lines 42-44].

As per claim 12, Liu discloses transmitting a plurality of data signals in parallel mode [Column 1, lines 46-47] from a first device (502) to a second device (506) over a first bus (504); detecting phase information of each data signal received at the second device (506) against a corresponding clock signal [Column 7, lines 46-47]; sending the phase information from the second device (506) to the first device [Column 7, lines 42-44]; and adjusting an output delay of each data signal at the first device (502) based on the phase information received from the second device [Column 7, lines 42-47].

As per claim 19, Liu discloses a computer system [Column 2, line 36] comprising a processor (112), a first component (502) coupled to the core, and a second component (506) coupled to the first component, wherein the first component transmits data words [Column 4, line17-19] to the second component (506) in parallel mode, each data word including a plurality of data bits, wherein the second component detects phase information of each data bit relative to a corresponding clock signal and feeds back the phase information of each data bit to the first

component [Column 7, lines 36-43], the first component adjusts an output delay of each data bit based on the phase information fed back from the second component [Column 7, lines 43-47].

As per claim 25, Liu discloses a method comprising of transmitting a plurality of data signals in parallel mode [Column 1, lines 46-47] from a first device (502) to a second device (506) over a first bus (504), detecting phase information of each data signal received at the second device (506) against a corresponding clock signal [Column 7, lines 46-47], sending the phase information from the second device to the first device [Column 7, lines 42-44], and adjusting an output delay of each data signal at the first device (502) based on the phase information received from the second device [Column 7, lines 42-47].

***Allowable Subject Matter***

Claims 2, 3, 6, 8, 13, 14, 16, 20, 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 2 and 13, the prior art fails to disclose or suggest that the second device feeds back the phase information to the first device in serial mode.

Regarding claims 3 and 20, the prior art fails to disclose or suggest that the second component feeds back the sampled data patterns to the first component.

Regarding claim 6, the prior art fails to disclose or suggest that the first device detects phase variations that are in excess of one bit of the sampled data fed back from the second device and shifts data bit positions between parallel data words to align phase variations that are in excess of one bit interval.

Regarding claim 8, the prior art fails to disclose or suggest that the second device transmits parallel data sample to the first device, subsequent to the sampling of the data signals.

Regarding claims 14 and 26, the prior art fails to disclose or suggest a method including: sampling and holding at the second device parallel data pattern received from the first device; feeding back the sampled data from the second device to the first device; recognizing, at the first device, phase variations that are in excess of one bit of the sampled data fed back from the second device; and shifting data bit positions between parallel words to align phase variations that are in excess of one bit interval.

Regarding claim 16, the prior art fails to disclose or suggest a method including sending a parallel data sample from the second device to the first device; and upon receiving the parallel data sample at the first device, comparing the parallel data sample with a programmed parallel data pattern.

Regarding claim 22, the prior art fails to disclose or suggest that the first component receives data words from the second component in parallel mode, each data word including a plurality of data bits, and wherein the first component detects phase information of each data bit relative to a corresponding clock signal and adjusts a delay of the respective data bit based on the phase information detected prior to sampling of the data bits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav S Amin whose telephone number is (571) 272-3821. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NA

REHANA PERVEEN
PRIMARY EXAMINER
11-1-04